DEAD-TIME COMPENSATION FOR 2-LEVEL VOLTAGE SOURCE INVERTERS BASED ON HARMONIC CURRENT CONTROLLERS

Thanh Lich Nguyen[*], Thanh Loan Pham[#]
[*]University of Transport and Communications
[#]Hanoi University of Mining and Geology

Abstract: This paper proposes a dead-time compensation method for 2-level voltage source inverters based on harmonic current controllers. The sixth harmonic of the stator current in the synchronous reference frame originated from the dead-time effect is attenuated by using current resonant controllers. The resonant controllers are connected in parallel with the conventional PI current regulator. The resonant controllers calculate a compensation voltage that is equal to the error voltage due to the dead-time, therefore the dead-time effect is mitigated. The proposed method is verified by simulation results.

Keywords: Dead-time compensation, resonant controller.

I. INTRODUCTION

Pulse width modulation (PWM) method is widely used in controlling voltage source inverters (VSI) due to its simplicity. However, the output voltage of the VSI contains harmonics because of the non-linear characteristic of the inverter. The most significant source of the voltage distortion at the low modulation index is the deadtime that is used to prevent the inverter short circuit. To deal with the nonlinear characteristics of the inverter, a variety of methods have already been presented [1]–[11]. In most scenarios, dead-time compensation methods are based on an average value theory. By these methods, the lost voltage due to the dead-time is averaged over an entire period, and the dead-time compensation is done by adding the correspondingly resultant value to the reference voltage of the inverter. However, the complexity of the techniques is increased along with a reduction of noise immunity at the zero-crossing points of the current due to the detection operation of the current polarity.

This paper proposes a method based on harmonic current controllers that can compensate for the voltage reduction caused by the dead-time. Apart from a successful dead-time compensation, this technique can be adaptive to the motor speed without the modifications of the hardware circuit. In addition, a design based on the root locus method is used to find out the gain K_R at each frequency.

II. THEORETICAL FUNDAMENTAL

According to [1], the dead time causes a voltage distortion in the phase voltages. In the synchronous reference frame, the voltage distortion in the d- and q-axis are given as follows:

$$v_{ds}^{DT} = \frac{4}{\pi}\Delta V\left\{\frac{12}{35}\sin 6\omega_e t + \frac{24}{143}\sin 12\omega_e t + \cdots\right\} \quad (1)$$

$$v_{qs}^{DT} = \frac{4}{\pi}\Delta V\left\{-1 + \frac{2}{35}\cos 6\omega_e t + \frac{2}{143}\cos 12\omega_e t + \cdots\right\} \quad (2)$$

where ω_e is the electrical angular velocity, the superscript "DT" corresponds to dead-time, the subscript "s" denotes the stator quantities, and

$$\Delta V = \frac{-T_d - t_{ON} + t_{OFF}}{2T_s} V_{dc}, \quad i_{as} > 0 \quad (3)$$

$$\Delta V = \frac{T_d + t_{ON} - t_{OFF}}{2T_s} V_{dc}, \quad i_{as} < 0 \quad (4)$$

with T_d, t_{ON}, t_{OFF} are the dead-time, turn on time and turn off time of the switches; T_s is the switching frequency of the current control loop.

The 6[th] harmonic in the d- and q-axis of the stator currents given in (1) and (2) creates the 6[th] harmonic in the corresponding current as follows:

$$i_{ds}^{DT} = \frac{4}{\pi}\Delta V\left\{\frac{12}{35Z_6}\sin(6\omega_e t + \varphi_6) + \frac{24}{143}\sin(12\omega_e t + \varphi_{12}) + \cdots\right\} \quad (5)$$

$$i_{qs}^{DT} = \frac{4}{\pi}\Delta V\left\{-\frac{1}{R_s} + \frac{2}{35Z_6}\cos(6\omega_e t + \varphi_6) + \frac{2}{143}\cos(12\omega_e t + \varphi_{12}) + \cdots\right\} \quad (6)$$

Contact author: Thanh Lich Nguyen
Email: lichnt@utc.edu.vn
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where $Z_k = \sqrt{R_s^2 + (k\omega_e L)^2}$ is the k^{th} impedance, φ_k is the phase angle corresponding to the k^{th} harmonic.

It is realized that the deadtime compensation is carried out by calculating the compensation voltage. It can be conducted based on the voltage path according to (1)-(2) or the current control loop according to (5)-(6). The compensation method can be conducted if the error voltage ΔV defined by (3)-(4) can be precisely calculated. However, the turn on time t_{ON} and turn off time t_{OFF} are difficult to be defined. Hence, the method based on the current control loop is preferred to the former one.

The idea behind the method based on the current control loop in the synchronous reference frame is to cancel the 6^{th} harmonic and its multiples. The output of the compensation algorithm is also the compensated voltage like (3)-(4). In [1], the authors proposed such a compensation technique, but it is complicated to be carried out as it requires some integrators, a phase-lock loop and the calculation of the harmonic compensation voltages.

In this paper, the harmonic voltage is calculated by a harmonic current controller whose topology and theoretical design will be presented in the following section.

III. HARMONIC CURRENT CONTROLLER FOR THE DEAD TIME COMPENSATION

The topology of the resonant current controller for dealing with the 6^{th} harmonic and its multiples in the stator currents is depicted in Figure 1. The resonant controller is in parallel with the conventional PI controller and is characterized by the fundamental frequency f_{r} and the gain K_{r}. The function of the PI controller is to cancel low frequency input noises while that of the resonant controller is to damp a specific harmonic in the input and/or the disturbance.

As the deadtime creates the 6^{th} and its multiples harmonics in the voltage, it can be modelled as a disturbance acting after the inverter, as it is shown in Figure 1. The effect of the resonant component will be analyzed in terms of disturbance rejection, meaning that the transfer function from the current to the voltage disturbance proposed by the dead time will be taken into account.

The Bode diagram from the current $i_{\mathrm{d}}(s)$ to the distortion voltage is depicted in Figure 2. In this example, the resonant frequency is set to $f_{\mathrm{r}} = 90\,Hz$, and $K_{\mathrm{R}} = 30000$. It can be seen that at the resonant frequency f_{r}, the gain of $G_{DT}(s)$ is very low. This means that the harmonic corresponding to f_{r} in the spectrum of $u_{DT}(s)$ has negligible effects on current i_{d}. In the case the resonant frequency f_{r} is chosen to be the multiple of the 6^{th} electrical frequency, those harmonics in the spectrum of the current will be cancelled. As a result, the effects of the dead-time and turn on/turn off time of the switches on the phase current are attenuated.

$$G_{DT}(s) = \frac{i_{\mathrm{d}}(s)}{u_{DT}(s)} \quad (7)$$

The remaining question is regarded as the design of the resonant current controller. As frequency f_{r} is the multiple of the 6^{th} electrical frequency, it will be automatically updated according to the operating speed of the machine. For the selection of the gain K_{R}, the root-locus plot will be adopted to realize how the poles of the closed-loop transfer function $G_{DT}(s)$ change according to K_{R}.

The characteristic equation of $G_{DT}(s)$ is as follows:

$$\begin{aligned} 0 = {} & T_{\mathrm{e}}T_{\mathrm{PWM}} \cdot s^5 + (T_{\mathrm{e}}+T_{\mathrm{PWM}}) \cdot s^4 \\ & + \left(K_{\mathrm{e}}K_{\mathrm{p}} + 1 + \omega_{\mathrm{m}}^2 T_{\mathrm{e}}T_{\mathrm{PWM}}\right) \cdot s^3 \\ & + (K_{\mathrm{e}}K_{\mathrm{i}} + \omega_{\mathrm{m}}^2(T_{\mathrm{e}} + T_{\mathrm{PWM}}) \\ & + K_{\mathrm{e}}K_{\mathrm{R}}) \cdot s^2 + \omega_{\mathrm{m}}^2\left(K_{\mathrm{e}}K_{\mathrm{p}} + 1\right) \cdot s \\ & + \omega_{\mathrm{m}}^2 K_{\mathrm{e}}K_{\mathrm{i}} \end{aligned} \quad (8)$$

where $\omega_{\mathrm{m}} = 2\pi f_{\mathrm{r}}$.

The root-locus plotting form is obtained by rearrange (8) in the following form:

$$0 = 1 + K_{\mathrm{R}} \cdot \frac{A(s)}{B(s)} \quad (9)$$

where

$$A(s) = K_{\mathrm{e}} \cdot s^2 \quad (10)$$

and

$$\begin{aligned} B(s) = {} & T_{\mathrm{e}}T_{\mathrm{PWM}} \cdot s^5 + (T_{\mathrm{e}}+T_{\mathrm{PWM}}) \cdot s^4 \\ & + \left(K_{\mathrm{e}}K_{\mathrm{p}} + 1 + \omega_{\mathrm{m}}^2 T_{\mathrm{e}}T_{\mathrm{PWM}}\right) \\ & \cdot s^3 \\ & + \left(K_{\mathrm{e}}K_{\mathrm{i}} + \omega_{\mathrm{m}}^2(T_{\mathrm{e}} + T_{\mathrm{PWM}})\right) \\ & \cdot s^2 + \omega_{\mathrm{m}}^2\left(K_{\mathrm{e}}K_{\mathrm{p}} + 1\right) \cdot s \\ & + \omega_{\mathrm{m}}^2 K_{\mathrm{e}}K_{\mathrm{i}} \end{aligned} \quad (11)$$

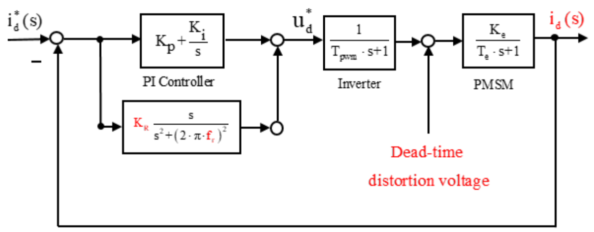

Figure 1. Control structure of the resonant current controller for dead-time compensation

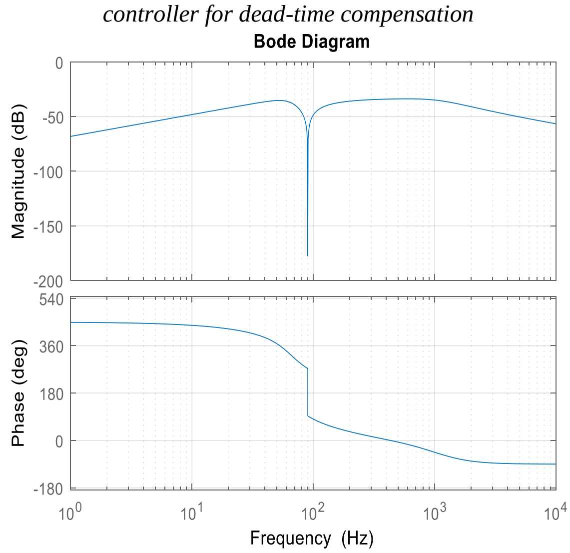

Figure 2. The Bode diagram from the current to the distortion voltage

The root locus of $G_{DT}(s)$ is shown in Figure 3 that depicts five segments corresponding to the locus of the five roots. Figure 4 shows the zoom-in that contains the dominant poles of $G_{DT}(s)$. From Figure 4, the gain K_R can be chosen to satisfy desired damping and overshoot of the closed loop system. This method can be applied for each frequency to be damped. The gain K_R at each frequency is obtained and is used to build a look-up table for implementing the resonant controller in the whole frequency range.

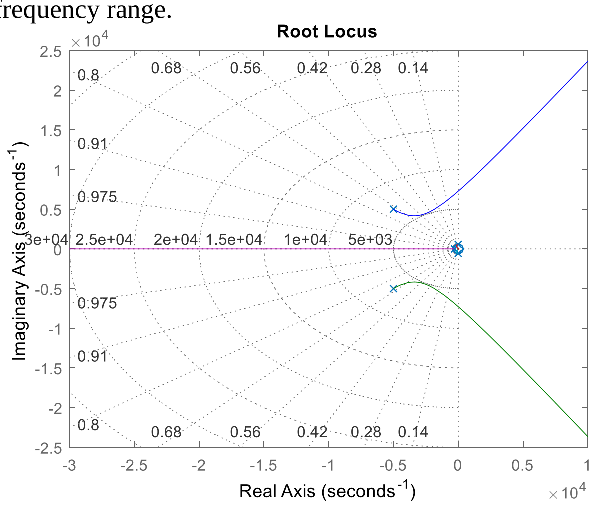

Figure 3. The root locus of the transfer function $G_{DT}(s)$

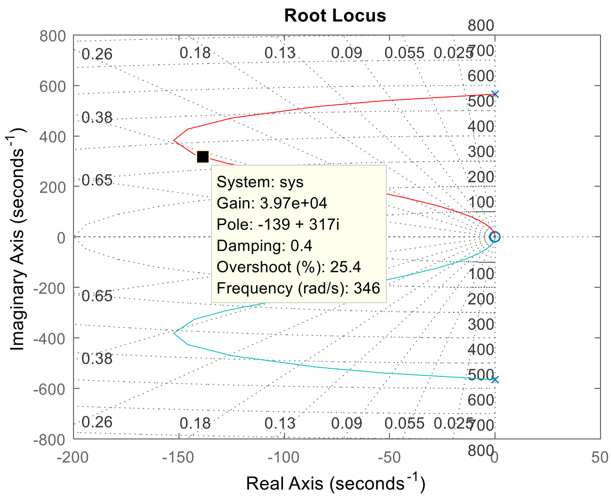

Figure 4. A zoom in of the root locus of the transfer function $G_{DT}(s)$

IV. SIMULATION VERIFICATION

A surface-mounted permanent magnet synchronous machine (SPMSM) is used to verify the effectiveness of the proposed compensation method. The core parameters of the simulation model are given in the following table:

Parameters	Values
Phase resistance	$R_s = 3.2\Omega$
Phase inductance	$L_d = L_q = 10.9$ mH
Rated torque	$T_N = 4.9$ Nm
Rated speed	$n_N = 3000$ Rpm
PWM sampling frequency	$f_{PWM} = 10$ kHz
Dead time	$T_{DT} = 2$ μs

Figure 5 shows currents i_a and i_d when the compensation algorithm is inactivated. The spectrum analysis of the i_a as depicted in Figure 6 confirms the fact that the harmonics of $(6k \pm 1)\omega_e$ are noticeable. This means that harmonics of $6k \cdot \omega_e$ are significant in the spectrum content of i_d. This phenomenon is coincident with the theoretical analysis as given in (5) and (6).

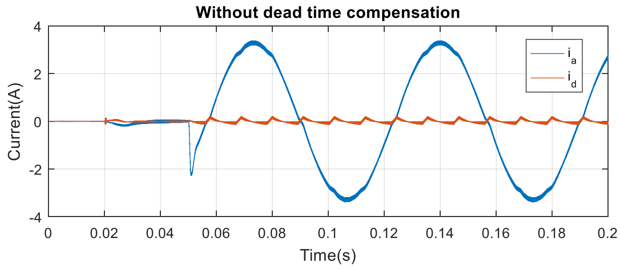

Figure 5. Current phase a and in the d-axis without dead time compensation

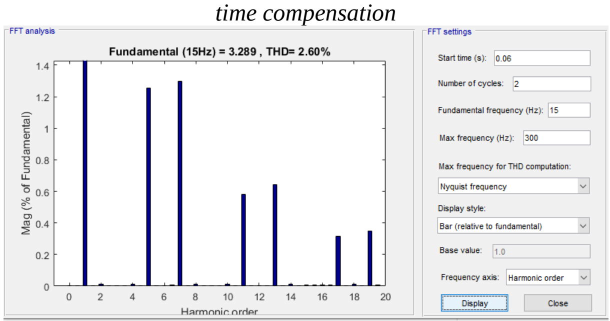

Figure 6. Harmonic orders of current phase a (i_a)

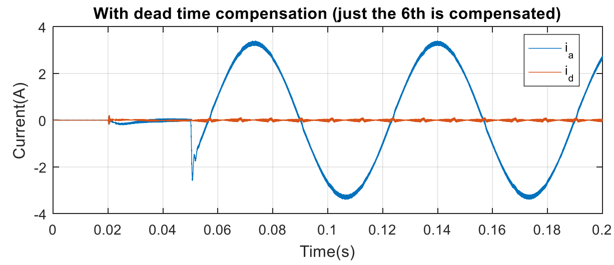

Figure 7. Currents with only the 6th harmonic compensation

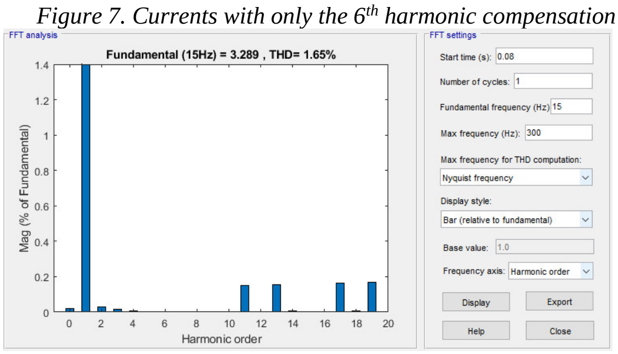

Figure 8. Harmonics current phase a while only the 6th harmonic is compensated

For the case where only the 6th harmonic is compensated, the corresponding results are shown in Figure 7 and Figure 8. It is observed in Figure 8 that harmonics according to the 5th and the 7th were significantly reduced, but the remaining harmonics are not decreased and even boosted up. The current distortion is still visible in both the phase current and the phase on the d-axis of the synchronous reference frame. The reason for this is that only the 6th is controlled. For a more precise dead-time compensation, more harmonics should be considered.

When the 12th harmonic in the d- and q-axis currents is considered along with the 6th, the results are shown in Figure 8 and Figure 9. The phase current depicted in Figure

8 is sinusoidal, meaning that the effect of the dead-time was reduced considerably. The fast Fourier transform (FFT) of the current as shown in Figure 9 demonstrates that the 5th, 7th, 11th and 13th are vanished and the functionality of the resonant controller is confirmed.

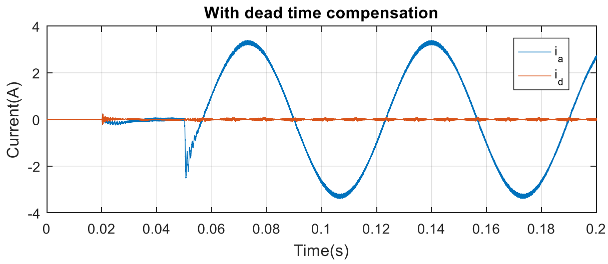

Figure 9. Currents with the 6th and 12th harmonics compensation

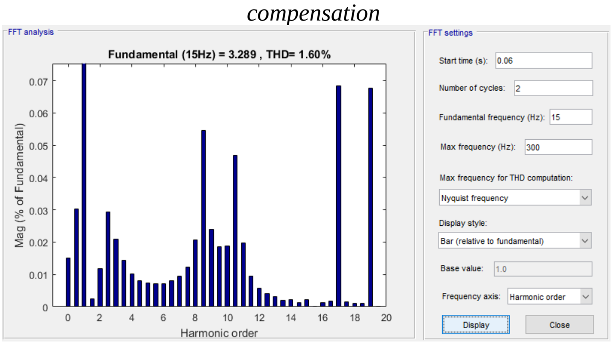

Figure 10. of the current FFT

V. CONCLUSIONS

A dead-time compensation technique based on harmonic current controllers was introduced in this paper. By a combination of the conventional PI current controller and the resonant controller, the sixth harmonic of the stator current in the synchronous reference frame was attenuated. Additionally, the dead-time effect was eliminated due to the resonant controller, in which the compensation voltage was computed to be equal to a reduction of voltage caused by dead-time. The effectiveness of the proposed method was verified by simulation results. The obtained results show
smooth transient responses of the output current during switching operation of semiconductor inside the inverter.

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BÙ THỜI GIAN AN TOÀN CHO BIẾN TẦN NGUỒN ÁP 2 MỨC DỰA TRÊN BỘ ĐIỀU KHIỂN ĐIỀU HÒA DÒNG ĐIỆN

Tóm tắt: Bài báo đề xuất phương pháp bù thời gian an toàn cho biến tần nguồn áp 2 mức dựa trên bộ điều khiển điều hòa dòng điện. Sóng hài bậc sáu của dòng điện stator trong hệ tọa độ tham chiếu đồng bộ gây ra bởi thời gian an toàn được suy giảm bằng cách dùng bộ điều khiển cộng hưởng. Bộ điều khiển cộng hưởng được mắc song song với bộ điều khiển tích phân tỷ lệ (PI) truyền thống. Bộ điều khiển cộng hưởng sẽ tính toán điện áp bù bằng điện áp bị giảm bởi thời gian an toàn, vì thế loại bỏ được sự ảnh hưởng của thời gian an toàn. Phương pháp đề xuất được kiểm nghiệm bởi các kết quả mô phỏng.

Từ khoá: Bù thời gian an toàn, bộ điều khiển cộng hưởng.

Thanh Lich Nguyen received the bachelor degree in electrical engineering from Hanoi University of Science and Technology, Hanoi, Vietnam in 2003 and the master degree in automation from Hanoi University of Mining and Geology, Hanoi, Vietnam in 2010, and the Ph.D degree in electrical engineering from Technical University of Darmstadt, Darmstadt, Germany in 2019. Currently, he is lecturer at University of Transport and Communications. His current research interests include power electronics, automation, mechatronics, renewable energy conversion systems and microgrid.

Thanh Loan Pham was born in Viet Nam in 1981. She received her B.Sc, M.Sc and Ph.D. in Electrical Engineering from Hanoi University of Science and Technology - HUST and Hanoi University of Mining and Geology – HUMG in 2003, 2005 and 2015, respectively. From 2003 to 2004, she was an automation engineer at Industrial Machinery and Instruments Holding Joint Stock Company. She joined the Automation Department, HUMG in 2004. Her research interests include Automation Control Theory, Modeling and Simulation and Process Control System.