A NUMERICAL SIMULATION DESIGN OF A THREE-MODE 3-DB POWER SPLITTER BASED ON SOI WAVEGUIDES FOR APPLICATIONS IN OVERLAPPING PHOTONIC NEURAL NETWORKS

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Abstract: In this paper, we present a numerical simulation design of a 1:2 power splitter optical circuit with an evenly distributed 50:50 splitting ratio for all three modes simultaneously. The proposed design is based on the SOI material platform with wafers having a silicon layer thickness of 220nm, in accordance with VLSI chip manufacturing technology standards. The entire geometric structure is optimized and the optical performance is evaluated using the 3D-BPM numerical simulation method. Simulation results show that the proposed structure exhibits low insertion loss (I.L) with variations of less than 5dB over a 100nm bandwidth. Additionally, the proposed structure demonstrates relatively high tolerance, corresponding to relative tolerances in width and height achieved as ΔW=±20nm and Δh=±10nm, respectively, with the overshoot of I.L not exceeding 1.5dB. The entire structure occupies a small integrated space of only 10μm x 50μm. These advantageous optical performance features lead to promising potential for photonic integrated circuits, particularly in applications aimed at constructing versatile functional components for large-scale photonic integrated circuits. Additionally, they also play a crucial role in establishing independently operational photonic neural networks utilizing broadband mode-division multiplexing (MDM) channelsKeywords – 3-dB coupler, three-mode, Ψ-junction, multimode interference coupler, silicon photonics, mode division multiplexing, photonic neural network.

Keywords: 3-dB splitter, simultaneous tree-mode, Ψ-junction, multimode interferometer, silicon photonics, photonic neural network, MDM technology.

I. INTRODUCTION

Inspired by parallel signal processing in the human brain and fueled by an explosion of data, AI has recently regained attention from researchers. Companies like Intel [1], IBM [2], and Google [3] have all prioritized AI as a vital strategic development direction. The explosive growth of AI is largely driven by deep learning [4] using artificial neural networks (ANNs). Neural network algorithms involve extensive multiplicative accumulation (MAC) operations, which traditional central processing units (CPUs) designed for the von Neumann architecture struggle to execute efficiently. In the von Neumann scheme, computation and signal processing memory are physically separated, and CPUs operate sequentially. This data flow between memory and the processor limits computational efficiency when conducting batch parallel signal processing. The one-size-fits-all approach is no longer viable for AI computing tasks. As a result, researchers are directing their focus toward new hardware architectures (such as graphics processing units (GPUs) and field programmable gate arrays (FPGAs)) specifically tailored to ANNs and deep learning. While GPUs, FPGAs, and even neuroelectronics like IBM TrueNorth [5] and Google TPU [3] have improved power efficiency and speed for inference tasks (learning), the decline of Moore's Law [6] has significantly impeded the further advancement of electronic microprocessors. The underlying power consumption and bandwidth limitations of electrical connections have become the primary bottlenecks in current AI hardware.

Due to cost and special fabrication requirements, the issue of mass-producing traditional discrete photonic devices poses considerable challenges. Similar to microelectronic hardware, improving computational performance for photonic chips also depends on an increasing number of devices. Fortunately, the advent of silicon photonics, compatible with standard complementary metal-oxide-semiconductor (CMOS) microelectronics integration technology, has paved the way for large-scale and reproducible fabrication of photonic chips. Silicon photonics technology employs both photons and electrons as 'information carriers,' enabling the integration of photonic structures with electronic devices on the same silicon substrate [7]. This integration results in a new chip with comprehensive functionalities required for rapid information processing.

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Natural silicon photonics offer the dual advantages of electronics and photonics, facilitating the integration and mass production of photonic devices on a scale similar to microelectronic chips, all while operating at the speed of light with minimal energy consumption. Although enhancing the integration density of photonic devices remains a formidable challenge, silicon photonics has witnessed substantial progress in recent years [8]. Mature CMOS integrated technology enhances the efficiency of photonic chip production while minimizing production costs.

Recently, the mode division multiplexing (MDM) technique [9], [10] has emerged as a promising solution alongside wavelength division multiplexing (WDM) to increase bandwidth capacity beyond the limits of Shannon's theorem [11], [12]. With the persistent and significant surge in data demand, high-density integration of silicon photonic components holds significant implications for achieving affordability, low power consumption, and high performance. Devices within an MDM-WDM hybrid system are employed to fulfill diverse functions and serve as key building blocks for constructing silicon-based chip-scale integrated photonic networks on insulators (SOIs), as well as future programmable photonic neural networks (PNNs) [13].

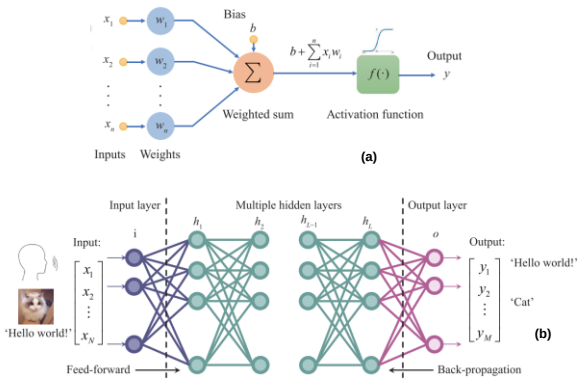

Figure 1. (a) An artificial neuron with a simple nonlinear model: showing inputs (x_1, x_2, . . . , x_n), their corresponding weights (w_1, w_2, . . . , w_n), bias b, and the nonlinear activation function f(x) applied to the weighted sum of input signals, the output connected to other neurons through synapses (connecting links), forming a neural network; (b) diagram of a multi-layer artificial neural network comprising an input layer, multiple hidden layers, and an output layer, the circles represent neurons, and each neuron is connected to all neurons in the next layer.

Certain MDM-WDM systems have demonstrated that guided modes can be treated as independent transmission channels in optical communication systems, especially for applications in data center systems or short-distance access optical communication systems [14], [15], such as PNNs or data center interconnection networks [16], [17].

In the realm of optical information processing and computing chips, the 50:50 power divider, commonly referred to as the 3-dB splitter, holds a crucial role. The function of the 3-dB division circuit can be observed in amplitude modulation or multilevel modulation mechanisms [18]–[20], optical switching in a 1×2 configuration achieved through directional couplers or Mach-Zehnder interference (MZI) configurations [21], and optical path protection switches in a 1:1 (cold-standby) or 1+1 (hot-standby with selectivity) configuration [22], as well as in optical level converters. Among these, directional couplers [23],[24], multimode interference [25], and adiabatic couplers [26] represent the three typical fundamental forms of 3-dB optical splitters.

However, the previously proposed splitters primarily support operation for single-mode optical signals. In this paper, we introduce a design for a 3-dB splitter capable of accommodating three conduction modes in a silicon photonics-based waveguide, holding potential applications for multilayer PNNs where each lattice is carried within an independent orthogonal mode. The research is founded on SOI materials that align with CMOS chip fabrication technology. The entire process of optimization and evaluation of optical properties is conducted through 3D-BPM numerical simulation.

II. OPERATION OF PHOTONIC NEURAL NETWORK AND THE ROLE OF THE 3-DB POWER SPLITTER

The rapid development of Artificial Neural Networks (ANNs) for AI tasks has led to the intensive exploration

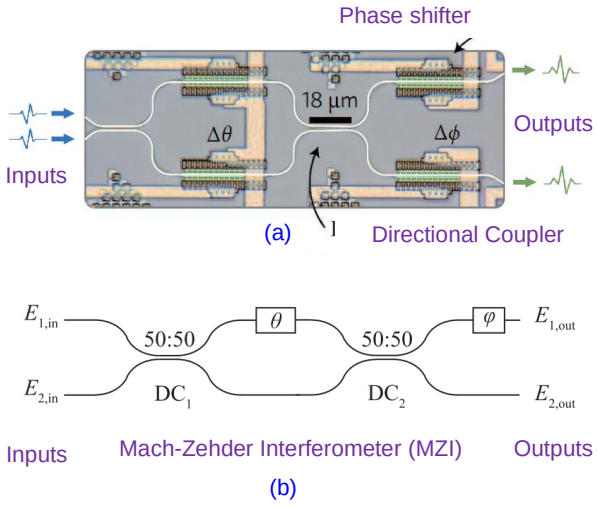

Figure 2. A Mach-Zehnder interferometer can be individually programmed with two thermo-optic phase shifters (a), illustrated diagram of a programmable MZI, consisting of a phase shifter (θ) between two variable 50:50 couplers, followed by another phase shifter (φ).

of efficient hardware implementations that mimic the natural processing capabilities of the brain. The neuron, depicted in Figure 1, serves as the fundamental functional unit of the human brain. Researchers are committed to comprehending the intricate functions of neurons and emulating their unparalleled energy efficiency. Figure 1(a) presents a basic illustration of an artificial neuron. This neuron comprises three primary components: Firstly, a weighted set of connections called synapses. The input signals (x_1, x_2, ..., x_n) are weighted according to their associated weights (w_1, w_2, ..., w_n). Secondly, the linear combinator, responsible for performing weighted additions. Lastly, a non-linear activation function $f(x)$,

typically monotonically bounded, is applied. The combined signals undergo a non-linear process before being emitted as output. The function f(x) serves the purpose of normalization, which prevents output divergence after multiple layers. Artificial neurons can be trained, as opposed to programmed, for computational tasks through exposure to extensive data —a process known as learning. Today, the combination of artificial neurons and 'deep learning algorithms' [27] has garnered substantial attention in academia and industry alike, primarily due to their utility in image recognition, language translation, decision-making problems, etc. [28].

Figure 1(b) illustrates a multilayer ANN comprising numerous interconnected artificial neurons. The connections between these neurons symbolize sets of weighted signals traversing the network. The input requires pre-processed and vectorized data, such as audio, images, and language. The input layer establishes connections with at least one hidden layer. Within each layer, the data undergoes linear processing, often involving matrix multiplication, followed by non-linear activation. Each neuron relays data to all neurons in the subsequent hidden layer until reaching the final output layer, which produces the ultimate outcome.

A cyclic topology implies the absence of feedback or loop connections within the network. Both the input and output layers serve as optical interfaces to the external world. ANNs can be effectively trained by introducing ample training data into the network and subsequently computing outputs through forward propagation. The weight parameters are then fine-tuned and adjusted using the standard back-propagation method [6].

The Mach-Zehnder interferometer is the most widely used interferometer in photonic integrated circuits. It finds significant application in modulating optical signals within these circuits by manipulating thermooptic phase shifters. A lossless phase-modulated MZI (depicted in Figure 2) with two symmetrical branches for optical beam separation, facilitating optical transformations, can be described using a 2×2 unit matrix U(2). The scattering matrix of a directional coupler (DC) is as follows:

$$DC = \begin{pmatrix} cos(\kappa L) & j\,sin(\kappa L) \\ j\,sin(\kappa L) & cos(\kappa L) \end{pmatrix} \quad (1)$$

Where κ is the coupling coefficient, L is the length of the coupling region, j is an imaginary number (j^2=-1) representing that the cross coupling through the directional coupler introduces a phase shift of π/2 upon request. With a 3-dB splitter (50:50), κL=π/4, and therefore, the unit matrix U(2) can be represented as:

$$U(2) = P_\varphi DC_2 P_\theta DC_1 = je^{j\theta/2}\begin{pmatrix} e^{j\varphi}\,sin(\theta/2) & e^{j\varphi}\,cos(\theta/2) \\ cos(\theta/2) & -sin(\theta/2) \end{pmatrix} \quad (2)$$

Here, P_φ and P_θ are phase shift operators, DC_1 and DC_2 are 50:50 directional couplers. The transformation matrix of the free unit U can be decomposed into basic matrices $U(2)$ by layering intercrossing Mach-Zehnder interferometers (MZIs), and the amplitude signal

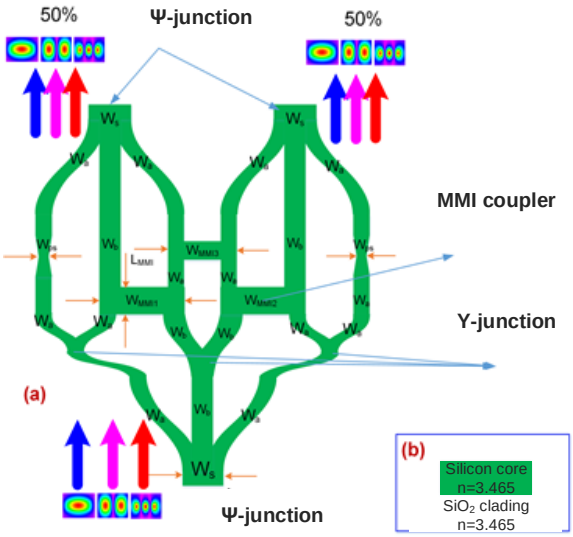

Figure 3. Structure of a 3-dB photonic mode splitter for three modes based on SOI material and channel waveguides: (a) top view, (b) side view.

relationship between input and output ends of light is determined by E_{out}=$U.E_{in}$.

Therefore, in a photonic neural network system, the elements playing the role of the 3-dB splitters are crucial basic components. In a photonic circuit system, if we consider each guided mode that is orthogonal to each other, carrying information from the inputs of a separate neural network, creating a mode division multiplexing system according to N modes (where N is a positive integer) will result in a superposition of N independent PNN networks that are integrated in the system simultaneously.

The subsequent part of the article will delve into the detailed presentation of an optical circuit design for a 3-dB splitter for three guided modes within waveguides operating simultaneously. This design is based on silicon photonics and holds potential applications for three independent PNN networks operating concurrently, with each network carried within an independent orthogonal mode [29].

III. STRUCTURE DESIGN AND OPERATION ANALYSIS

A. Structural description and general operation principle

The structural diagram of the 3-dB photonic mode splitter for three guided modes within optical waveguides is depicted in Figure 3. The waveguide structure consists of a configuration of waveguides in a 1:2 symmetrical arrangement. This structure includes an input waveguide branch in the form of a Ψ-junction coupler, resembling a three-fingered nail head, with its root being a multi-mode-supporting waveguide segment for the operation of three modes under TE (transverse electric) polarization, with a root width (stem width) denoted as W_s.

The design involves three identical Ψ-junction coupler structures, one serving as an input and two as output

branches. The device employs three Y-junction couplers to divide the branches and three sets of 2×2 multimode interference couplers (MMI) through a multimode interference mechanism in a 2×2 configuration, denoted as $3L_\pi$. The optical device employs two phase shifters with a required phase shift angle of π to generate an appropriate optical signal combination in order to recreate all three modes as desired, with a power splitting ratio of 50:50. The core of the waveguide employs silicon material (Si), a silicon dioxide (SiO_2) glass cladding layer, and is designed to operate for three TE modes with a central operational wavelength of λ=1550nm.

This waveguide structure is widely applied as a standard in the modern design of devices and integrated photonic circuits. This is due to two reasons: firstly, they are fabricated from a standard silicon-on-insulator (SOI) wafer with a thickness of 220 nm, commonly used in electronic integrated circuit manufacturing to produce VLSI chips; secondly, with a thickness of 220 nm, the photonic modes can only be guided in the width direction (higher order modes cannot be guided along the height direction of the silicon core layer) under TE polarization and an operating wavelength of 1550 nm. Therefore, in photonic design, waveguides made from standard SOI wafers (220 nm thickness) are utilized.

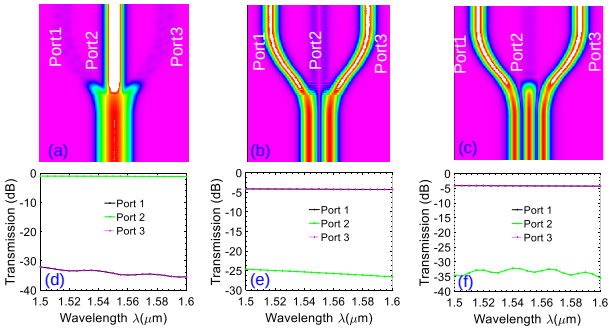

Figure 4. Electric field distribution characteristics and optical responses in terms of wavelength response when passing through the Ψ-junction coupler: (a, d) for TE_0 mode, (b, e) for TE_1 mode, and (c, f) for TE_2 mode.

In this design, the optical mode splitter is constructed in the form of channel waveguides (for the convenience of mask fabrication in the production process), with a silicon core layer and a silicon dioxide glass cladding layer having corresponding refractive indices n_r=3.465 and n_c=1.445 at a wavelength of 1550 nm. The entire waveguide structure can be fabricated using modern optical lithography methods, such as electron beam writing and dry etching using inductively coupled plasma (ICP) etching [30], or ultraviolet photolithography (DUV lithography) with a channel height of 220 nm from a standard SOI wafer (with a high 220 nm silicon core layer).

B. Ψ-junction coupler

The stem and two output ports form a symmetric Ψ-junction, where the body of the Ψ-junction connects to a waveguide that supports the transmission of three orthogonally guided modes. To support these three modes, the effective width W_s falls within the range of 0.7μm ÷ 1.2μm. In this design, the width W_s is chosen to be 1 μm to support the operation of the three modes based on TE polarization, which are commonly used modes in the waveguide of photonic integrated circuits, including TE_0, TE_1, and TE_2. This is explained by the fact that the TE modes guided in the waveguide are manufactured from a standard SOI (silicon-on-insulator) wafer with a thickness of 220nm, which is utilized for VLSI chip production using CMOS technology. Additionally, noted that TE modes only exist in the lateral dimension of the waveguide, while in the vertical dimension, only single mode can be existed. Subsequently, this waveguide is combined with three other waveguides. The central waveguide is a straight waveguide with a width of W_b = 0.5μm and a length of L_s = 120μm, while the two symmetric side waveguides take the form of sinusoidal-bent waveguides (also known as S-bent waveguides) with a width of W_a = 0.4μm, and corresponding lateral length and width denoted as L_s and G = 1.6μm. The Ψ-junction coupler enables mode selection based on appropriate waveguide mode-matching conditions: mode TE_0 travels through the central waveguide, while mode TE_1 and mode TE_2 propagate towards the two symmetric branches. This is demonstrated through simulation results obtained using the three-dimensional beam propagation method (3D-BPM). The simulated optical characteristics reveal a broad 100-nm bandwidth response that almost maintains the transmission properties of the designed Ψ-junction coupler, as illustrated in Figure 4.

C. Y-junction coupler and 2×2 multimode interference coupler

To achieve the balanced separation of TE_0, TE_1, and TE_2 orthogonal modes in a 50:50 ratio (3-dB coupler), a Y-junction is employed. This Y-junction consists of two symmetric sinusoidal-shaped branches and is combined with a multimode interference coupler (MMI) [31]. The input signal at the Y-junction is divided symmetrically. The middle point of the Y-junction is connected to the central waveguide of a trident coupler with waveguide widths denoted as Wb, while the two sinusoidal-shaped branches (S-bent waveguides) of the Ψ-junction are connected to each other. The width of the Y-junction waveguides is denoted as W_a. The combination of the two branches of the Y-junction, each having widths of W_a and W_b, forms a 2×2 MMI1 coupler with a width of W_{MMI1} = 2.05μm, and the remaining branch is similarly connected to a 2×2 MMI2 coupler. These two 2×2 MMIs are symmetric in terms of their dimensions (that means W_{MMI1} = W_{MMI2}= 2.05μm), as seen in Figure 1. The remaining branch of the Y-junction is connected to a phase shifter. Next, the outputs of the first and second 2×2 MMIs in this layer are connected to two waveguides with widths of W_a and W_b to obtain the reflected images. These two waveguides then pass through two 2×2 MMIs in the first layer and are subsequently connected to a 2×2 MMI3 coupler in the second layer, with input and output branch widths both being W_a. The width of the second-layer MMI is W_{MMI3} = 1.7μm.

The operation of the proposed 2×2 MMI coupler follows the Talbot interference effect [32]. In the general

interference mechanism (GI) [33]–[35], the amplitude and phase of the signal through the MMI coupler change based on the length of the MMI and the input-output positions of the access waveguides (single-mode) for the MMI waveguide coupler. According to the theory of multimode interference, the reflected image of the 2×2 MMI coupler (which plays the role of a cross-coupler) has a length of LMMI = 3Lπ, where Lπ is half the beat length, meaning a π-radian phase shift, calculated using the following formula [32]:

$$L_\pi = \frac{4n_{eff}W_e^2}{3\lambda} \quad (3)$$

where

$$W_e = W_{MMI} + \frac{\lambda}{\pi}\left(n_{eff}^2 - n_c^2\right)^{-0.5} \quad (4)$$

Here, W_e is the effective mode width calculated based on the depth of field of the TE mode, λ is the operating wavelength, n_{eff} is the effective refractive index of the core layer, and n_c is the refractive index of the cladding layer. To enhance transmission efficiency across modes, linearly tapered waveguides have been placed to connect with waveguides before and after coupling with the MMI.

We use BPM simulations to optimize the lengths L_{MMI} of MMI couplers to achieve the desired self-imaging quality when passing through each corresponding multimode interference coupler. By combining equations (3) and (4), we calculate the optimal MMI lengths and best achievable transmissions via the scanning progress of numerical parameters to find out the optimal values of the half-beat lengths of MMI couplers as $L_{\pi MMI1} = L_{\pi MMI2} =$ 33.5µm and $L_{\pi MMI3}$ = 23.25µm, respectively.

D. Phase shifter

The phase shifter (PS) is utilized to modulate the phase variations in the optical paths to a specific value, ensuring that when combining optical signals from the same source interfere constructively to recreate the original signal shape during transmission. Through the two 2×2 MMIs, (with the same frequency and polarization), they will the signals are phase-shifted by π compared to the initial signals, as passing through each 2×2 MMI with a length of $3L_\pi$ results in a phase shift of π/2 (due to the signal division into two branches) compared to the input signal. To restore the initial signal, we have additionally connected both branches to a phase shifter with ΔΦ = π to re-balance the phase when recombining the optical paths at the final output.

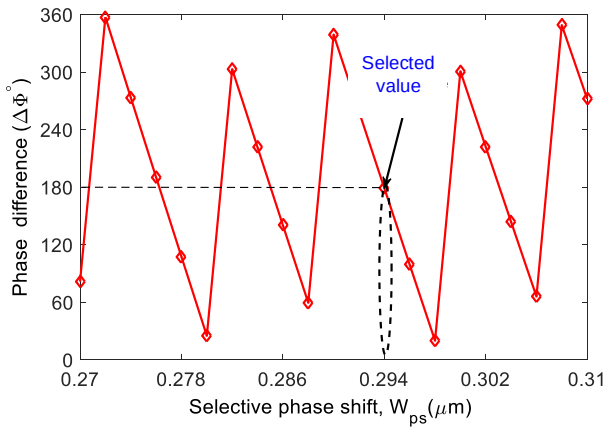

Figure 5. Simulation results for selecting the width of the phase shifter to achieve a phase shift of π radians.

In this article, the phase shifter is designed as a butterfly-shaped waveguide to generate passive phase shifters used in the structural diagram in Figure 1. The length of the phase shifter is L_{ps} = 51.75µm, and the width is W_a = 0.4µm. The phase of the PS continuously changes according to the variation of the butterfly wing section Wps. The phase variation on the PS is calculated using the following formula:

$$\Delta\Phi\left(z_0, z_0 + L_{ps}\right) = \int_{z_0}^{z_0+L_{ps}} \left(\beta_0 - \beta_{ps}(z)\right)dz \quad (5)$$

Where z_0 and $z_0 + L_{ps}$ are respectively the starting and ending positions of the phase shifter along the propagation direction z, β0 is the propagation constant starting from z0, and βps(z) is a function of the propagation constant at the point z around the range (z_0, $z_0 + L_{ps}$). According to BPM simulation, in Figure 5, we can clearly observe the significant change of the phase shifter with respect to Wps. At W_{ps} = 0.294µm = 294nm the phase shift is ΔΦ = π.

IV. SIMULATION RESULTS AND DISCUSSION

Firstly, we simulate the mode transmission to realize the channel separation function for analyzing the transmission results of each TE mode. Figure 6 illustrates the results through BPM simulations by displaying the electric field envelope distribution of the corresponding TE_0, TE_1, and TE_2 modes, each with a 50:50 ratio as proposed by the device's design at the operating wavelength of 1550nm. The results exhibit conformity with the operational analysis of the device mentioned above, with only a minor insignificant radiative leakage from the core to the cladding.

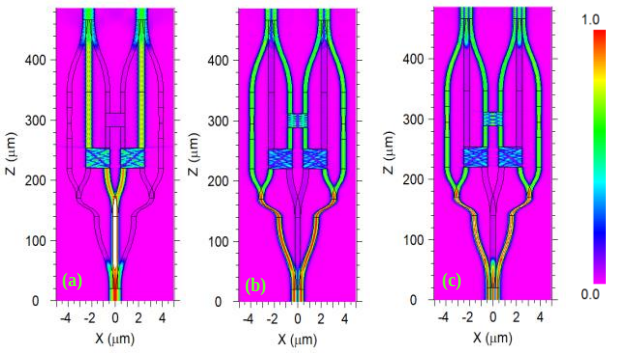

Figure 6. Contour maps illustrating the electric field envelope for the proposed 3-dB mode division multiplexer: (a), (b), and (c) correspond to the three modes TE0, TE1, and TE2, respectively, in a 50:50 ratio.

To characterize the optical performance of the device, we evaluate the parameter I.L. (insertion loss) computed using the following formula:

$$I.L. = 10 log_{10}\left(\frac{P_{out}}{P_{in}}\right) \quad (6)$$

In which, P_{in} represents the input power of the waveguide normalized by 1 unit of power at the input, and P_{out} is the desired power obtained at the output.

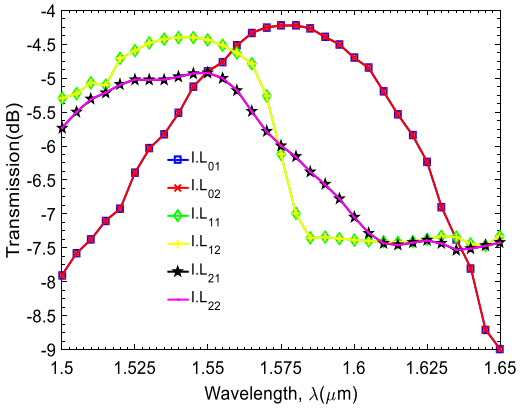

Figure 7. Optical performance characteristics of the device depend on the operating wavelength for the three modes in a 50:50 splitting ratio.

Next, we will evaluate the operational bandwidth of the proposed device using the parameter *I.L.mn* where *m*=0,1,2 represents the mode order and *n*=1,2 corresponds to the left and right outputs of the device. The 3D-BPM simulation results over a wavelength range of 1.5µm-1.65µm reveal that, for the 50:50 ratio, I.L exhibits fluctuations below 9dB for all three modes. Among them, TE_1 and TE_2 modes exhibit their peak at around 1550nm, while TE_0 and TE1 modes have peak responses at wavelengths of 1575nm-1.6nm, as shown in Figure 7.

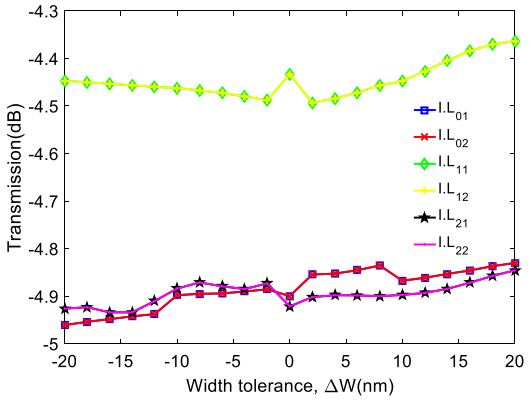

Figure 8. Simulation results of the transmission characteristics of the coupler with input waveguide width variation ΔW (nm) satisfying the optimal point of splitting and mode conversion at a 50:50 ratio.

Manufacturing tolerances play a crucial role in the device's performance, as all fabrication processes introduce losses. In simulation-based studies, it is essential to evaluate fabrication losses to assess the system's efficiency. The height of the waveguide is set according to the height of the silicon-guiding layer in the standard

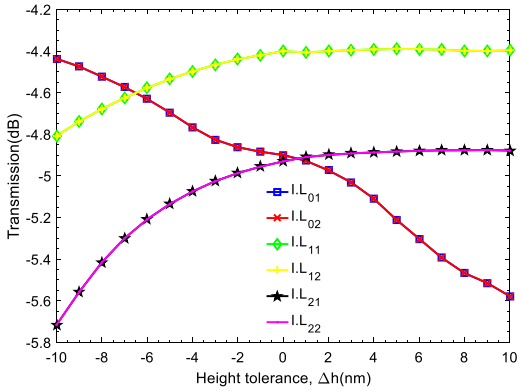

Figure 9. Simulation results of the transmission characteristics of the coupler as a function of the vertical height mismatch Δh (nm) satisfying the optimal point for splitting and mode division in a 50:50 ratio.

220nm SOI waveguide. In practice, the quality of the SOI wafer, used in both general VLSI integrated circuit manufacturing and specifically in photonic chips, depends on the wafer supplier's specifications. Similarly, the accuracy of the achieved waveguide width relies on the Ebeam or DUV lithography techniques. Likewise, the precision of the simulated design depends on the accuracy of the simulation model. Therefore, we must investigate fabrication tolerances for the waveguide width and height. Regarding the fabrication tolerance in the waveguide width ΔW, the performance evaluation is depicted in Figure 8, showing the optical performance variations within the ±20nm width range. For the 50:50 ratio, it is observed that the insertion loss of TE_1 mode is less than the insertion loss of TE_0 mode, and the insertion loss of TE_2 mode is less than 5dB, with peak fluctuations ranging from 4.3dB to 5dB.

Subsequently, we investigated the variations in the waveguide height Δh (nm) within the range of ±10nm, as depicted in Figure 9. For the 50:50 ratio, TE_1 and TE_2 modes exhibit decreasing curves, and their graphs are parallel to each other; when Δh is 0nm, the graph saturates. As Δh increases, TE_0 mode insertion loss also increases, oscillating between 4.4dB and 5.8dB. The observations indicate that varying the waveguide width within ±20nm and the waveguide height within ±10nm yields favorable insertion loss results, with minor fluctuations in the range of approximately 1.5dB within the studied tolerance range.

The entire proposed structure is confined within a compact integration area, within the rectangular footprint of 10µm×500µm = 5000µm^2, as seen throughout the simulation results in Figure 4. Such a compact size, coupled with its excellent optical characteristics regarding insertion loss across a wide spectral range of 100nm (from 1500nm to 1600nm), demonstrates the potential of the device to function as a mode division signal processing device for MDM technology and next-generation high-speed broadband optical communication systems.

V.CONCLUSION

The article presents a proposed design for an equal splitter 3-dB optical circuit for three orthogonal guided modes based on photonic technology and the SOI material platform. The device relies on Ψ-junction coupler structures, sinusoidal waveguides, and multimode interference couplers as fundamental components of the integrated circuit built on the Silic photonic technology. The optimization of the design and evaluation of optical characteristics are performed through 3D-BPM numerical simulations. The simulation results demonstrate that the mode division structure operates with low insertion loss and significant fabrication tolerances within a wide spectral range. Additionally, the compact integrated design holds promising potential for extensive applications in large-scale integrated photonic circuits and independent stacked photonic neural networks with high-density mode-division multiplexing.

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THIẾT KẾ MÔ PHỎNG SỐ HỌC CỦA BỘ CHIA CÔNG SUẤT 3-DB BA MODE DỰA TRÊN ỐNG DẪN SÓNG SOI CHO ỨNG DỤNG TRONG MẠNG NƠRON QUANG HỌC XẾP CHỒNG

Tóm tắt – Trong bài báo này, chúng tôi trình bày một thiết kế mô phỏng số của vi mạch quang tử chia công suất 1:2 với tỷ lệ chia 50:50 đều nhau cho cả ba mode đồng thời. Cấu trúc được đề xuất thiết kế dựa trên nền tảng vật liệu SOI với phiến có độ dày lớp silic là 220nm theo tiêu chuẩn của công nghệ chế tạo vi mạch VLSI. Toàn bộ cấu trúc hình học được tối ưu hóa và đánh giá hiệu năng quang học được thực hiện qua phương pháp mô phỏng số 3D-BPM. Kết quả mô phỏng cho thấy cấu trúc đề xuất có suy hao chèn I.L thấp với sự biến động nhỏ hơn 5dB trong khoảng rộng 100nm. Bên cạnh đó, cấu trúc đề xuất có dung sai tương đối cao tương ứng với mức dung sai theo chiều rộng và chiều cao đạt được là ΔW=±20nm và Δh= ±10nm với sự thăng giáng của I.L không vượt quá 1.5dB. Toàn bộ cấu trúc chỉ tiêu tốn không gian tích hợp nhỏ 10μm×50μm. Những ưu điểm về hiệu năng quang học do đó đưa đến tiềm năng hứa hẹn của vi mạch quang trong các ứng dụng để xây dựng các thành phần xử lý chức năng đa dạng của vi mạch tích hợp quang tử cỡ lớn, cũng như xây dựng các mạng nơ ron quang tử xếp chồng bởi sự ghép kênh phân chia theo mode (MDM) băng rộng.

Từ khóa – bộ chia 3-dB, ba mode đồng thời, tiếp giáp chữ Ψ, bộ ghép giao thoa đa mode, quang tử silic, mạng nơ ron quang tử, công nghệ MDM.

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